1. A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer to completely fill said opening;

forming a buffer zone on a surface of said copper layer; and

depositing a capping layer overlying said copper layer and said buffer zone to complete said copper metallization in said fabrication of said integrated circuit device.

2. The method according to Claim 1 further comprising forming semiconductor device structures in and on said substrate wherein said semiconductor device structures include gate electrodes, source/drain regions, and lower level metallization.

3. The method according to Claim 2 wherein said opening is made to one of said semiconductor device structures within said substrate.

4. The method according to Claim 1 wherein said depositing said capping layer is an in-situ process.

5. The method according to Claim 1 wherein said step of forming said copper layer is selected from the group consisting of: physical vapor deposition, chemical vapor deposition, electroplating, and electroless plating.

6. The method according to Claim 1 wherein said step of forming said buffer zone comprises applying F ions or controlled corrosion gas to said copper surface.

7. The method according to Claim 1 wherein said capping layer is selected from the group consisting of silicon nitride and silicon carbide and wherein said capping layer has a thickness of between about 200 and 1000 Angstroms.

8. A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer to completely fill said opening; and

applying F ions to said copper layer to form a buffer zone on a surface of said copper layer and in-situ depositing a capping layer overlying said copper

layer to complete said copper metallization in said fabrication of said integrated circuit device.

9. The method according to Claim 8 further comprising forming semiconductor device structures in and on said substrate wherein said semiconductor device structures include gate electrodes, source/drain regions, and lower level metallization.

10. The method according to Claim 9 wherein said opening is made to one of said semiconductor device structures within said substrate.

11. The method according to Claim 8 wherein said step of forming said copper layer is selected from the group consisting of: physical vapor deposition, chemical vapor deposition, electroplating, and electroless plating.

12. The method according to Claim 8 wherein said step of applying F ions to said copper layer comprises treating said copper with NF_3 plasma.

13. The method according to Claim 8 wherein said capping layer is selected from the group consisting of silicon nitride and silicon carbide and wherein said capping

layer has a thickness of between about 200 and 1000 Angstroms.

14. A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing an opening through a dielectric layer overlying a substrate on a wafer;

forming a copper layer to completely fill said opening wherein copper oxide forms naturally on a surface of said copper layer; and

applying F ions to said copper layer wherein said F ions remove said copper oxide and form a buffer zone on a surface of said copper layer and in-situ depositing a capping layer overlying said copper layer to complete said copper metallization in said fabrication of said integrated circuit device.

15. The method according to Claim 14 further comprising forming semiconductor device structures in and on said substrate wherein said semiconductor device structures include gate electrodes, source/drain regions, and lower level metallization.

16. The method according to Claim 15 wherein said opening is made to one of said semiconductor device

structures within said substrate.

17. The method according to Claim 14 wherein said step of forming said copper layer is selected from the group consisting of: physical vapor deposition, chemical vapor deposition, electroplating, and electroless plating.

18. The method according to Claim 14 wherein said step of applying F ions to said copper layer comprises treating said copper with NF_3 plasma.

19. The method according to Claim 14 wherein said buffer zone transfers thermal vertical strain in said copper to horizontal strain thereby preventing formation of copper hillocks.

20. The method according to Claim 14 wherein said capping layer is selected from the group consisting of silicon nitride and silicon carbide and wherein said capping layer has a thickness of between about 200 and 1000 Angstroms.